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IEEE STD	IEEE Standard

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1. **CMOS imager design for fast centroid readout**
Thomas, C.; Hornsey, R.; Yip, K.;
Electrical and Computer Engineering, 2004. Canadian Conference on
Volume 4, 2-5 May 2004 Page(s):2315 - 2318 Vol.4
AbstractPlus | Full Text: PDF(362 KB) IEEE CNF

2. **A simplicial CNN architecture for on-chip image processing**
Mandolesi, P.S.; Julian, P.; Andreou, A.G.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International
Volume 3, 23-26 May 2004 Page(s):III - 29-32 Vol.3
Digital Object Identifier 10.1109/ISCAS.2004.1328675
AbstractPlus | Full Text: PDF(288 KB) IEEE CNF

3. **Mixed analog-digital image processing circuit based on Hamming artificia architecture**
Badel, S.; Schmid, A.; Leblebici, Y.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International
Volume 5, 23-26 May 2004 Page(s):V-780 - V-783 Vol.5
AbstractPlus | Full Text: PDF(678 KB) IEEE CNF

4. **Programmable multi-task on-chip processing for CMOS imagers**
Boussaid, F.; BermakA; Bouzerdoum, A.;
MEMS, NANO and Smart Systems, 2003. Proceedings. International Conferen
20-23 July 2003 Page(s):227 - 232
AbstractPlus | Full Text: PDF(630 KB) IEEE CNF

5. **Computing ADC harmonic content from a reduced number of values**
Sousa Mendonca, H.; Machado da Silva, J.; Silva Matos, J.;
Instrumentation and Measurement Technology Conference, 2003. IMTC '03. P
20th IEEE
Volume 2, 20-22 May 2003 Page(s):1217 - 1220 vol.2
AbstractPlus | Full Text: PDF(337 KB) IEEE CNF

6. **Application-specific computing with adaptive register file architectures**
Sangireddy, R.; Somani, A.K.;
Application-Specific Systems, Architectures, and Processors, 2003. Proceedin
International Conference on

24-26 June 2003 Page(s):183 - 192

AbstractPlus | Full Text: PDF(1207 KB) IEEE CNF

☐ **7. Shunting inhibition-based on-chip processing for CMOS imagers**
Boussaid, F.; Bermak, A.; Bouzerdoum, A.;
Neural Information Processing, 2002. ICONIP '02. Proceedings of the 9th Inter
Conference on
Volume 3, 18-22 Nov. 2002 Page(s):1310 - 1314 vol.3

AbstractPlus | Full Text: PDF(374 KB) IEEE CNF

☐ **8. Hardware support for real-time embedded multiprocessor system-on-a-cl management**
Shalan, M.; Mooney, V.J., III;
Hardware/Software Codesign, 2002. CODES 2002. Proceedings of the Tenth I
Symposium on
6-8 May 2002 Page(s):79 - 84
Digital Object Identifier 10.1109/CODES.2002.1003605

AbstractPlus | Full Text: PDF(438 KB) IEEE CNF

☑ **9. A 256×256 pixel smart CMOS image sensor for line-based stereo vision a**
Ni, Y.; Guan, J.;
Solid-State Circuits, IEEE Journal of
Volume 35, Issue 7, July 2000 Page(s):1055 - 1061
Digital Object Identifier 10.1109/4.848217

AbstractPlus | References | Full Text: PDF(244 KB) IEEE JNL

☑ **10. A 256×256-pixel smart CMOS image sensor for line based stereo vision a**
Yang Ni; Guan, J.H.;
Solid-State Circuits Conference, 1999. ESSCIRC '99. Proceedings of the 25th
21-23 Sept. 1999 Page(s):258 - 261

AbstractPlus | Full Text: PDF(408 KB) IEEE CNF

☑ **11. Smart vision sensors**
Gokstorp, M.; Forchheimer, R.;
Image Processing, 1998. ICIP 98. Proceedings. 1998 International Conference
Volume 1, 4-7 Oct. 1998 Page(s):479 - 482 vol.1
Digital Object Identifier 10.1109/ICIP.1998.723537

AbstractPlus | Full Text: PDF(296 KB) IEEE CNF

☑ **12. A gesture controlled human interface using an artificial retina chip**
Miyake, Y.; Freeman, W.T.; Ohta, J.; Tanaka, K.; Kyuma, K.;
Lasers and Electro-Optics Society Annual Meeting, 1996. LEOS 96., IEEE
Volume 1, 18-19 Nov. 1996 Page(s):292 - 293 vol.1
Digital Object Identifier 10.1109/LEOS.1996.565247

AbstractPlus | Full Text: PDF(212 KB) IEEE CNF

☑ **13. Superconducting infrared detector arrays with integrated processing circ**
Osterman, D.P.; Marr, P.; Dang, H.; Yao, C.-T.; Radparvar, M.;
Magnetics, IEEE Transactions on
Volume 27, Issue 2, Part 4, Mar 1991 Page(s):2681 - 2684
Digital Object Identifier 10.1109/20.133764

AbstractPlus | Full Text: PDF(360 KB) IEEE JNL

[redacted]

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1. **A 500-dpi AC capacitive hybrid flip-chip CMOS ASIC/sensor module for fi navigation, and pointer detection with on-chip data processing**
Vermesan, O.; Riisnaes, K.H.; Le Pailleur, L.; Nysaether, J.B.; Bauge, M.; Rus S.; Blystad, L.-C.; Grindvoll, H.; Pedersen, R.; Pezzani, R.; Kaire, D.;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 12, Dec 2003 Page(s):2288 - 2296
Digital Object Identifier 10.1109/JSSC.2003.819175
AbstractPlus | Full Text: PDF(734 KB) IEEE JNL

2. **A dynamically reconfigurable monolithic CMOS pressure sensor for smai**
Sergio, M.; Manaresi, N.; Campi, F.; Canegallo, R.; Tartagni, M.; Guerrieri, R.;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 6, June 2003 Page(s):966 - 975
Digital Object Identifier 10.1109/JSSC.2003.811977
AbstractPlus | References | Full Text: PDF(1180 KB) IEEE JNL

3. **First fully integrated 2-D array of single-photon detectors in standard CM**
Rochas, A.; Gosch, M.; Serov, A.; Besse, P.A.; Popovic, R.S.; Lasser, T.; Rigle
Photonics Technology Letters, IEEE
Volume 15, Issue 7, July 2003 Page(s):963 - 965
Digital Object Identifier 10.1109/LPT.2003.813387
AbstractPlus | References | Full Text: PDF(411 KB) IEEE JNL

4. **Employing logic-enhanced memory for high-performance ATM network ir**
Agusleo, H.; Soparkar, N.;
High Performance Distributed Computing, 1996., Proceedings of 5th IEEE Inte Symposium on
6-9 Aug. 1996 Page(s):192 - 200
AbstractPlus | Full Text: PDF(636 KB) IEEE CNF

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Dynamically partitioned test scheduling with adaptive TAM configuration constrained SoC testing**
Zhao, D.; Upadhyaya, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 24, Issue 6, June 2005 Page(s):956 - 965
Digital Object Identifier 10.1109/TCAD.2005.847893
Abstract | Full Text: PDF(632 KB) **IEEE JNL**

2. **Implementation of a 4 /spl times/ 4 switch with passive interconnects**
Hashimoto, Y.; Yorozu, S.; Kameda, Y.; Fujimaki, A.; Terai, H.; Yoshikawa, N.;
Applied Superconductivity, IEEE Transactions on
Volume 15, Issue 2, Part 1, June 2005 Page(s):356 - 359
Digital Object Identifier 10.1109/TASC.2005.849835
Abstract | Full Text: PDF(864 KB) **IEEE JNL**

3. **High-resolution flash time-to-digital conversion and calibration for syster testing**
Levine, P.M.; Roberts, G.W.;
Computers and Digital Techniques, IEE Proceedings-
Volume 152, Issue 3, 6 May 2005 Page(s):415 - 426
Digital Object Identifier 10.1049/ip-cdt:20045063
Abstract | Full Text: PDF(616 KB) **IEE JNL**

4. **Energy minimization for hybrid BIST in a system-on-chip test environmer**
Ubar, R.; Shchenova, T.; Jervan, G.; Peng, Z.;
Test Symposium, 2005. European
22-25 May 2005 Page(s):2 - 7
Digital Object Identifier 10.1109/ETS.2005.16
Abstract | Full Text: PDF(248 KB) **IEEE CNF**

5. **Proceedings. European Test Symposium. ETS 2005**
Test Symposium, 2005. European
22-25 May 2005
Digital Object Identifier 10.1109/ETS.2005.18
Full Text: PDF(344 KB) **IEEE CNF**

6. **Test scheduling for modular SOCs in an abort-on-fail environment**

Ingelsson, U.; Goel, S.K.; Larsson, E.; Marinissen, E.J.;
Test Symposium, 2005. European
22-25 May 2005 Page(s):8 - 13
Digital Object Identifier 10.1109/ETS.2005.38

Abstract | Full Text: PDF(208 KB) IEEE CNF

7. **Using data compression in automatic test equipment for system-on-chip**
Karimi, F.; Navabi, Z.; Meleis, W.M.; Lombardi, F.;
Instrumentation and Measurement, IEEE Transactions on
Volume 53, Issue 2, April 2004 Page(s):308 - 317
Digital Object Identifier 10.1109/TIM.2003.822703

Abstract | Full Text: PDF(688 KB) IEEE JNL

8. **Design of front-end circuit for Superconductive A/D converter and demor operation up to 43 GHz**
Furuta, F.; Saitoh, K.; Takagi, K.;
Applied Superconductivity, IEEE Transactions on
Volume 14, Issue 1, March 2004 Page(s):40 - 45
Digital Object Identifier 10.1109/TASC.2004.824343

Abstract | Full Text: PDF(536 KB) IEEE JNL

9. **SOC-B design and testing technique of IS-95C CDMA transmitter for mea electric field intensity using FPGA and ASIC**
Kim, C.; Mike Myung-ok Lee; Byung-Lok Cho; Eshraghian, K.;
Electronic Design, Test and Applications, 2004. DELTA 2004. Second IEEE In Workshop on
28-30 Jan. 2004 Page(s):251 - 254
Digital Object Identifier 10.1109/DELTA.2004.10062

Abstract | Full Text: PDF(240 KB) IEEE CNF

10. **A user-configurable framework for testing prototype system-on-chip imp**
Manjikian, N.; Cordeiro, N.;
Circuits and Systems, 2004. NEWCAS 2004. The 2nd Annual IEEE Northeast
20-23 June 2004 Page(s):341 - 344
Digital Object Identifier 10.1109/NEWCAS.2004.1359102

Abstract | Full Text: PDF(523 KB) IEEE CNF

11. **Practical test architecture optimization for system-on-a-chip under floorp constraints**
Sugihara, M.; Murakami, K.; Matsunaga, Y.;
VLSI, 2004. Proceedings. IEEE Computer society Annual Symposium on
19-20 Feb. 2004 Page(s):179 - 184

Abstract | Full Text: PDF(273 KB) IEEE CNF

12. **Infrastructure for modular SOC testing**
Marinissen, E.J.; Waayers, T.;
Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004
3-6 Oct. 2004 Page(s):671 - 678

Abstract | Full Text: PDF(1177 KB) IEEE CNF

13. **Session MB1: On-Chip Testing of Embedded Silicon Transducers**
SOC Conference, 2004. Proceedings. IEEE International
12-15 Sept. 2004 Page(s):11 - 11
Digital Object Identifier 10.1109/SOCC.2004.1362332

Full Text: PDF(155 KB) IEEE CNF

14. **A current sensor for on-chip, non-intrusive testing of RF systems**
Soldo, A.; Gopalan, A.; Mukund, P.R.; Margala, M.;

VLSI Design, 2004. Proceedings. 17th International Conference on
2004 Page(s):1023 - 1026
Digital Object Identifier 10.1109/ICVD.2004.1261064

Abstract | Full Text: PDF(5503 KB) IEEE CNF

☐ **15. Frequency synthesizer for on-chip testing and automated tuning**
Valero-Lopez, A.Y.; Valdes-Garcia, A.; Sanchez-Sinencio, E.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International
Volume 4, 23-26 May 2004 Page(s):IV - 565-8 Vol.4

Abstract | Full Text: PDF(321 KB) IEEE CNF

☐ **16. On-chip testing of embedded silicon transducers**
Mir, S.; Charlot, B.; Rufer, L.; Courtois, B.;
SOC Conference, 2004. Proceedings. IEEE International
12-15 Sept. 2004 Page(s):13 - 18
Digital Object Identifier 10.1109/SOCC.2004.1362334

Abstract | Full Text: PDF(609 KB) IEEE CNF

☐ **17. On-chip testing of embedded silicon transducers**
Mir, S.; Rufer, L.; Charlot, B.; Courtois, B.;
Microelectronics, 2004. ICM 2004 Proceedings. The 16th International Confere
6-8 Dec. 2004 Page(s):2 - 7
Digital Object Identifier 10.1109/ICM.2004.1434190

Abstract | Full Text: PDF(438 KB) IEEE CNF

☐ **18. Digital and analog system testing: fundamentals and new challenges**
Renovell, M.;
Microelectronics, 2004. ICM 2004 Proceedings. The 16th International Confere
6-8 Dec. 2004 Page(s):8 - 10
Digital Object Identifier 10.1109/ICM.2004.1434191

Abstract | Full Text: PDF(145 KB) IEEE CNF

☐ **19. On-chip testing of embedded transducers**
Mir, S.; Rufer, L.; Courtois, B.;
VLSI Design, 2004. Proceedings. 17th International Conference on
2004 Page(s):463 - 472
Digital Object Identifier 10.1109/ICVD.2004.1260965

Abstract | Full Text: PDF(1693 KB) IEEE CNF

☐ **20. High-speed operation of demultiplexer up to 56 GHz**
Furuta, F.; Saitoh, K.; Takagi, K.;
Applied Superconductivity, IEEE Transactions on
Volume 13, Issue 2, Part 1, June 2003 Page(s):567 - 570
Digital Object Identifier 10.1109/TASC.2003.813948

Abstract | Full Text: PDF(540 KB) IEEE JNL

☐ **21. An evaluation of built-in vs. off-chip strategies for online transient curren**
Alorda, B.; Segura, J.;
On-Line Testing Symposium, 2003. IOLTS 2003. 9th IEEE
7-9 July 2003 Page(s):178 - 182

Abstract | Full Text: PDF(685 KB) IEEE CNF

☐ **22. An efficient approach to SoC wrapper design, TAM configuration and tes**
Pouget, J.; Larsson, E.; Peng, Z.; Flottes, M.-L.; Rouzeyre, B.;
European Test Workshop, 2003. Proceedings. The Eighth IEEE
25-28 May 2003 Page(s):51 - 56

Abstract | Full Text: PDF(604 KB) IEEE CNF

☐ **23. On-chip testing of MEMS using pseudo-random test sequences**
Rufer, L.; Mir, S.; Simeu, E.; Domingues, C.;
Design, Test, Integration and Packaging of MEMS/MOEMS 2003. Symposium
5-7 May 2003 Page(s):50 - 55
Digital Object Identifier 10.1109/DTIP.2003.1287007
Abstract | Full Text: PDF(1597 KB) IEEE CNF

☐ **24. BIT for intelligent system design and condition monitoring**
Gao, R.X.; Suryavanshi, A.;
Instrumentation and Measurement, IEEE Transactions on
Volume 51, Issue 5, Oct. 2002 Page(s):1061 - 1067
Digital Object Identifier 10.1109/TIM.2002.807796
Abstract | Full Text: PDF(575 KB) IEEE JNL

☐ **25. An efficient BIST method for distributed small buffers**
Jone, W.B.; Huang, D.C.; Wu, S.C.; Lee, K.J.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 10, Issue 4, Aug. 2002 Page(s):512 - 515
Digital Object Identifier 10.1109/TVLSI.2002.800532
Abstract | Full Text: PDF(288 KB) IEEE JNL

☐ **26. Native mode functional self-test generation for Systems-on-Chip**
Jayaraman, K.; Vedula, V.M.; Abraham, J.A.;
Quality Electronic Design, 2002. Proceedings. International Symposium on
18-21 March 2002 Page(s):280 - 285
Digital Object Identifier 10.1109/ISQED.2002.996752
Abstract | Full Text: PDF(232 KB) IEEE CNF

☐ **27. On using rectangle packing for SOC wrapper/TAM co-optimization**
Iyengar, V.; Chakrabarty, K.; Marinissen, E.J.;
VLSI Test Symposium, 2002. (VTS 2002). Proceedings 20th IEEE
28 April-2 May 2002 Page(s):253 - 258
Digital Object Identifier 10.1109/VTS.2002.1011146
Abstract | Full Text: PDF(379 KB) IEEE CNF

☐ **28. Formulation of SOC test scheduling as a network transportation problem**
Koranne, S.; Choudhary, V.S.;
Design, Automation and Test in Europe Conference and Exhibition, 2002. Proc
4-8 March 2002 Page(s):1125
Digital Object Identifier 10.1109/DATE.2002.998481
Abstract | Full Text: PDF(249 KB) IEEE CNF

☐ **29. Data compression for system-on-chip testing using ATE**
Karimi, F.; Meleis, W.; Navabi, Z.; Lombardi, F.;
Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 1
International Symposium on
6-8 Nov. 2002 Page(s):166 - 174
Digital Object Identifier 10.1109/DFTVS.2002.1173513
Abstract | Full Text: PDF(912 KB) IEEE CNF

☐ **30. Proceedings of the 11 th Asian test symposium (ATS'02)**
Test Symposium, 2002. (ATS '02). Proceedings of the 11th Asian
18-20 Nov. 2002 Page(s):i - x
Digital Object Identifier 10.1109/ATS.2002.1181675
Abstract | Full Text: PDF(368 KB) IEEE CNF

☐ **31. 60 Gbps throughput demonstration of an asynchronous SFQ-pulse arbitr**

Yorozu, S.; Kameda, Y.; Tahara, S.;
Applied Superconductivity, IEEE Transactions on
Volume 11, Issue 1, Part 1, March 2001 Page(s):621 - 624
Digital Object Identifier 10.1109/77.919421

Abstract | Full Text: PDF(360 KB) IEEE JNL

☐ **32. Demonstration of 17 GHz operation of M-code generator based on SFQ w latch**
Akahori, A.; Takeuchi, N.; Mori, N.; Suzuki, Y.; Furuta, F.; Fujimaki, A.; Hayaka
Applied Superconductivity, IEEE Transactions on
Volume 11, Issue 1, Part 1, March 2001 Page(s):521 - 524
Digital Object Identifier 10.1109/77.919397

Abstract | Full Text: PDF(360 KB) IEEE JNL

☐ **33. Simultaneous reduction in volume of test data and power dissipation for chip**
Rosinger, P.; Gonciari, P.T.; Al-Hashimi, B.M.; Nicolici, N.;
Electronics Letters
Volume 37, Issue 24, 22 Nov. 2001 Page(s):1434 - 1436
Digital Object Identifier 10.1049/el:20010981

Abstract | Full Text: PDF(377 KB) IEE JNL

☐ **34. Use of the oscillation based built-in self-test method for smart sensor de**
Hodge, A.; Newcomb, R.; Hefner, A.;
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Sympc
Volume 2, 6-9 May 2001 Page(s):281 - 284 vol. 2
Digital Object Identifier 10.1109/ISCAS.2001.921062

Abstract | Full Text: PDF(436 KB) IEEE CNF

☐ **35. Fast test cost calculation for hybrid BIST in digital systems**
Orasson, E.; Raidma, R.; Ubar, R.; Jervan, G.; Peng, Z.;
Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on
4-6 Sept. 2001 Page(s):318 - 325
Digital Object Identifier 10.1109/DSD.2001.952315

Abstract | Full Text: PDF(640 KB) IEEE CNF

☑ **36. A low-cost adaptive ramp generator for analog BIST applications**
Azais, F.; Bernard, S.; Bertrand, Y.; Michel, X.; Renovell, M.;
VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001
29 April-3 May 2001 Page(s):266 - 271
Digital Object Identifier 10.1109/VTS.2001.923449

Abstract | Full Text: PDF(516 KB) IEEE CNF

☐ **37. Experimental evaluation of on-chip measurement of charge transfer by X**
Lal, K.; Hartnagel, H.L.; Goswami, N.; Thoma, P.;
Electronics Letters
Volume 36, Issue 14, 6 July 2000 Page(s):1204 - 1205
Digital Object Identifier 10.1049/el:20000892

Abstract | Full Text: PDF(164 KB) IEE JNL

☐ **38. An ILP formulation to optimize test access mechanism in system-on-chip**
Nourani, M.; Papachristou, C.;
Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):902 - 910
Digital Object Identifier 10.1109/TEST.2000.894301

Abstract | Full Text: PDF(680 KB) IEEE CNF

39. Test cost minimization for hybrid BIST

☐ Jervan, G.; Peng, Z.; Ubar, R.;
Defect and Fault Tolerance in VLSI Systems, 2000. Proceedings. IEEE Interna
Symposium on
25-27 Oct. 2000 Page(s):283 - 291
Digital Object Identifier 10.1109/DFTVS.2000.887168

Abstract | Full Text: PDF(496 KB) IEEE CNF

☐ **40. Clock-driven on-chip testing for superconductor logic circuits**
Hashimoto, Y.; Yorozu, S.; Numata, H.; Tahara, S.;
Applied Superconductivity, IEEE Transactions on
Volume 9, Issue 2, Part 3, June 1999 Page(s):3169 - 3172
Digital Object Identifier 10.1109/77.783702

Abstract | Full Text: PDF(396 KB) IEEE JNL

☐ **41. A fully integrated 16-channel RSFQ autocorrelator operating at 11 GHz**
Rylyakov, A.V.; Schneider, D.F.; Polyakov, Yu.A.;
Applied Superconductivity, IEEE Transactions on
Volume 9, Issue 2, Part 3, June 1999 Page(s):3623 - 3627
Digital Object Identifier 10.1109/77.783813

Abstract | Full Text: PDF(528 KB) IEEE JNL

☐ **42. A high-speed built-in-self-test design for DRAMs**
Shi-Yu Huang; Ding-Ming Kwai;
VLSI Technology, Systems, and Applications, 1999. International Symposium
8-10 June 1999 Page(s):50 - 53
Digital Object Identifier 10.1109/VTSA.1999.785997

Abstract | Full Text: PDF(300 KB) IEEE CNF

☐ **43. Auto-calibrating analog timer for on-chip testing**
Provost, B.; Sanchez-Sinencio, E.;
Test Conference, 1999. Proceedings. International
28-30 Sept. 1999 Page(s):541 - 548
Digital Object Identifier 10.1109/TEST.1999.805778

Abstract | Full Text: PDF(612 KB) IEEE CNF

☐ **44. Adaptive analog timer for on-chip testing**
Provost, B.; Sanchez-Sinencio, E.;
Design of Mixed-Mode Integrated Circuits and Applications, 1999. Third Intern
on
26-28 July 1999 Page(s):29 - 32
Digital Object Identifier 10.1109/MMICA.1999.833587

Abstract | Full Text: PDF(364 KB) IEEE CNF

☐ **45. On chip testing data converters using static parameters**
Arabi, K.; Kaminska, B.; Sawan, M.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 6, Issue 3, Sept. 1998 Page(s):409 - 419
Digital Object Identifier 10.1109/92.711312

Abstract | Full Text: PDF(260 KB) IEEE JNL

☐ **46. Proceedings. 16th IEEE VLSI Test Symposium (Cat. No.98TB100231)**
VLSI Test Symposium, 1998. Proceedings. 16th IEEE
26-30 April 1998
Digital Object Identifier 10.1109/VTEST.1998.671406

Abstract | Full Text: PDF(668 KB) IEEE CNF

☐ **47. Micro tensile-test system fabricated on a single crystal silicon chip**
Sato, K.; Shikida, M.; Yamasaki, M.; Yoshioka, T.;

Micro Electro Mechanical Systems, 1996, MEMS '96, Proceedings. 'An Investi
Structures, Sensors, Actuators, Machines and Systems'. IEEE, The Ninth Anni
Workshop on
11-15 Feb. 1996 Page(s):360 - 364
Digital Object Identifier 10.1109/MEMSYS.1996.494008

Abstract | Full Text: PDF(584 KB) IEEE CNF

☐ **48. Self-learning signature analysis for non-volatile memory testing**
Olivo, P.; Dalpasso, M.;
Test Conference, 1996. Proceedings., International
20-25 Oct. 1996 Page(s):303 - 308
Digital Object Identifier 10.1109/TEST.1996.556975

Abstract | Full Text: PDF(492 KB) IEEE CNF

☐ **49. Approaches to on-chip testing of mixed signal macros in ASICs**
Cobley, R.A.;
European Design and Test Conference, 1996. ED&TC 96. Proceedings
11-14 March 1996 Page(s):553 - 557
Digital Object Identifier 10.1109/EDTC.1996.494355

Abstract | Full Text: PDF(396 KB) IEEE CNF

☐ **50. An efficient 175 MHz programmable FIR digital filter**
Khoo, K.-Y.; Kwentus, A.; Willson, A.N., Jr.;
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium
3-6 May 1993 Page(s):72 - 75 vol.1
Digital Object Identifier 10.1109/ISCAS.1993.393660

Abstract | Full Text: PDF(252 KB) IEEE CNF

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1 Thermal Modeling, Characterization and Management of On-Chip Networks
Li Shang, Li-Shiuan Peh, Amit Kumar, Niraj K. Jha
December 2004 **Proceedings of the 37th annual International Symposium on Microarchitecture**
Full text available: pdf(551.38 KB) Additional Information: full citation, abstract

Due to the wire delay constraints in deep submicron technology and increasing demand for on-chip bandwidth, networks are becoming the pervasive interconnect fabric to connect processing elements on chip. With ever-increasing power density and cooling costs, the thermal impact of on-chip networks needs to be urgently addressed. In this work, we first characterize the thermal profile of the MIT Raw chip. Our study shows networks having comparable thermal impact as the processing elements and contr ...

2 A scalable, clustered SMT processor for digital signal processing
Mladen Berekovic, Sören Moch, Peter Pirsch
June 2004 **ACM SIGARCH Computer Architecture News**, Volume 32 Issue 3
Full text available: pdf(356.32 KB) Additional Information: full citation, abstract, references

A scalable, distributed, processor architecture is presented that emphasizes on high performance computing for digital signal processing applications by combining high frequency design techniques with a very high degree of parallel processing on a chip. The architecture is based on a superscalar processor model with a modified Tomasulo scheme [1], that was extended to eliminate all central control structures for the data flow and to support simultaneous instruction issue from multiple independen ...

3 CAD: Design and optimization of MOS current mode logic for parameter variations
Hassan Hassan, Mohab Anis, Mohamed Elmasry
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**
Full text available: pdf(304.83 KB) Additional Information: full citation, abstract, references, index terms

An automated optimization-based design strategy is proposed for single-level MOS Current Mode Logic (MCML) gates to overcome the complexities of the gate design procedure. The proposed design methodology determines the values of the design variables that achieve the minimum power dissipation point while attaining the required performance. The proposed design methodology has the advantage of speed, accuracy, and ability to include a large number of parameters in the design problem. Moreover, a fo ...

Keywords: MCML, automation, design, optimization, technology scaling, variation

4 Design styles (invited): Placement driven synthesis case studies on two sets of two chips: hierarchical and flat

Peter J. Osler

April 2004 **Proceedings of the 2004 international symposium on Physical design**

Full text available: pdf(299.92 KB) Additional Information: full citation, abstract, index terms

In this paper I describe two sets of two large ASIC chips that have recently been processed from netlist to final design by the Semi-Custom Design Team part of IBM's World-Wide Design Center. I address issues such as why the parts were selected for special handling, the issues with the designs that required custom engineering, and the special techniques used in placement driven synthesis that enabled successful completion of the designs.

Keywords: application specific integrated circuit (ASIC), netlist, placement, register transfer level (RTL), static timing analysis (STA), synthesis

5 Hardware/Software Co-testing of Embedded Memories in Complex SOCs

Bai Hong Fang, Qiang Xu, Nicola Nicolici

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(145.29 KB) Additional Information: full citation, abstract, index terms

A novel approach for testing embedded memories in complexsystems-on-a-chip (SOCs) is presented. The proposedsolution aims to balance the usage of the existing on-chipresources and dedicated design for test (DFT) hardwaresuch that the functional power constraints are not exceededduring test while trading-off the testing time againstDFT area and performance overhead. The suitability ofsoftware-centric and hardware-centric approaches for embeddedmemory testing is examined and to combine the advanta ...

6 Design space exploration and architectural design of HW/SW systems: Hardware support for real-time embedded multiprocessor system-on-a-chip memory management

Mohamed Shalan, Vincent J. Mooney

May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**

Full text available: pdf(533.74 KB) Additional Information: full citation, abstract, references, index terms, review

The aggressive evolution of the semiconductor industry --- smaller process geometries, higher densities, and greater chip complexity --- has provided design engineers the means to create complex high-performance Systems-on-a-Chip (SoC) designs. Such SoC designs typically have more than one processor and huge memory, all on the same chip. Dealing with the global on- chip memory allocation/de-allocation in a dynamic yet deterministic way is an important issue for the upcoming billion transistor mu ...

Keywords: Atalanta, SoCDMMU, System-on-a-Chip, dynamic memory management, embedded systems, real-time operating systems., real-time systems, two-level memory management

7 A reconfigurable multi-function computing cache architecture

Hue-Sung Kim, Arun K. Somani, Akhilesh Tyagi

February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**

Full text available: pdf(992.08 KB) Additional Information: full citation, abstract, references, citings, index terms

A considerable portion of a chip is dedicated to a cache memory in a modern microprocessor chip. However, some applications may not actively need all the cache storage, especially the computing bandwidth limited applications. Instead, such applications may be able to use some additional computing resources. If the unused portion of the cache could serve these computation needs, the on-chip resources would be utilized more efficiently. This presents an opportunity to explore the reconfigurat ...

8 Converting a 64b PowerPC processor from CMOS bulk to SOI technology
D. Allen, D. Behrends, B. Stanisic
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(90.91 KB) Additional Information: full citation, references, citings, index terms

9 Microservers: a new memory semantics for massively parallel computing
Jay B. Brockman, Peter M. Kogge, Thomas L. Sterling, Vincent W. Freeh, Shannon K. Kuntz
May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.40 MB) Additional Information: full citation, references, citings, index terms

Keywords: massively parallel, microserver, processing-in-memory

10 Built-in self-test methodology for A/D converters
R. de Vries, T. Zwemstra, E. M. J. G. Bruls, P. P. L. Regtien
March 1997 **Proceedings of the 1997 European conference on Design and Test**

Full text available: pdf(632.08 KB) Publisher Site Additional Information: full citation, abstract, citings

A (partial) Built-in Self-Test (BIST) methodology is proposed for analog to digital (A/D) converters. In this methodology the number of bits of the A/D converter that needs to be monitored externally in a test is reduced. This reduction depends, among other things, on the frequency of the applied test signal. At low test signal frequencies only the least significant bit (LSB) needs to be monitored and a "full" BIST becomes feasible. An analysis is made of the trade-off between the size of the on ...

Keywords: A/D converters, ADC testing, BIST methodology, analogue-digital conversion, built-in self-test, least significant bit, onchip test circuitry, test signal frequencies

11 Memory bandwidth limitations of future microprocessors
Doug Burger, James R. Goodman, Alain Kägi
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2

Full text available: pdf(1.60 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper makes the case that pin bandwidth will be a critical consideration for future microprocessors. We show that many of the techniques used to tolerate growing memory latencies do so at the expense of increased bandwidth requirements. Using a decomposition of execution time, we show that for modern processors that employ aggressive memory latency tolerance techniques, wasted cycles due to insufficient bandwidth generally exceed those due to raw memory latencies. Given the importance of ma ...

12 A laboratory for teaching parallel computing on parallel structures

Lan Jin, Lan Yang

March 1995 **ACM SIGCSE Bulletin , Proceedings of the twenty-sixth SIGCSE technical symposium on Computer science education**, Volume 27 Issue 1

Full text available: pdf(541.68 KB) Additional Information: full citation, abstract, references, citings, index terms

For the effective use of a laboratory for teaching parallel processing, it is desirable to have parallel systems that can implement various parallel structures at hardware or software level. Such systems developed in our laboratories are described in this paper. They are a multi-computer with reconfiguration and the PVM (Parallel Virtual Machine) with structural implementation. The paper proposes a methodology and several classes of problems for teaching message-passing programming on paral ...

13 A fast and flexible performance simulator for micro-architecture trade-off analysis on UltraSPARC-I

Marc Tremblay, Guillermo Maturana, Atsushi Inoue, Les Kohn

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(70.91 KB) Additional Information: full citation, references, citings, index terms

14 Simulation of a pyramid processor

Duane R. Ball, Gerard C. Blais, David Schaefer, Gregory Wilcox, R. Neil Wagoner

December 1985 **Proceedings of the 17th conference on Winter simulation**

Full text available: pdf(434.39 KB) Additional Information: full citation, abstract, references

This paper describes a simulation model of the MPP Pyramid [1] that has been constructed at the George Mason University. This model has been designed to facilitate experiments in processor control and in instruction set design.

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Relevance scale

21 A novel scan architecture for power-efficient, rapid test
Ozgur Sinanoglu, Alex Orailoglu
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(106.20 KB) Additional Information: full citation, abstract, references, citings, index terms

Scan-based testing methodologies remedy the testability problem of sequential circuits; yet they suffer from prolonged test time and excessive test power due to numerous shift operations. The high density of the unspecified bits in test data enables the utilization of the test response data captured in the scan chain for the generation of the subsequent test stimulus, thus reducing both test time and test data volume. The proposed scan-based test scheme accesses only a subset of scan cells for l ...

22 Designing SoCs for yield improvement: Embedding infrastructure IP for SOC yield improvement
Yervant Zorian
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(220.88 KB) Additional Information: full citation, abstract, references, citings, index terms

In addition to the functional IP cores, today's SOC necessitates embedding a special family of IP blocks, called Infrastructure IP blocks. These are meant to ensure the manufacturability of the SOC and to achieve adequate levels of yield and reliability. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This paper analyzes the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitate ...

Keywords: embedded test & repair, semiconductor IP, test resource partitioning, yield optimization

23 Test cost reduction for SOCS: Wrapper/TAM co-optimization, constraint-driven test scheduling, and tester data volume reduction for SOCs
Vikram Iyengar, Krishnendu Chakrabarty, Erik Jan Marinissen
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(168.08 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes an integrated framework for plug-and-play SOC test automation. This framework is based on a new approach for wrapper/TAM co optimization based on rectangle packing. We first tailor TAM widths to each core's test data needs. We then use rectangle packing to develop an integrated scheduling algorithm that incorporates precedence and power constraints in the test schedule, while allowing the SOC integrator to designate a group of tests as preemptable. Finally, we study the rela ...

24 New test methods targeting non-classical faults: Embedded software-based self-testing for SoC design

A. Krstic, W. C. Lai, K. T. Cheng, L. Chen, S. Dey
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(324.94 KB) Additional Information: full citation, abstract, references, index terms

At-speed testing of high-speed circuits is becoming increasingly difficult with external testers due to the growing gap between design and tester performance, growing cost of high-performance testers and increasing yield loss caused by inherent tester inaccuracy. Therefore, empowering the chip to test itself seems like a natural solution. Hardware-based self-testing techniques have limitations due to performance and area overhead and problems caused by the application of non-functional patterns. ...

Keywords: SoC test, VLSI test, functional test, microprocessor test

25 Testing and Fault-Tolerance: Minimizing concurrent test time in SoC's by balancing resource usage

Dan Zhao, Shambhu Upadhyaya, Martin Margala
April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(87.90 KB) Additional Information: full citation, abstract, references, index terms

We present a novel test scheduling algorithm for embedded core-based SoC's. Given a system integrated with a set of cores and a set of test resources, we select a test for each core from a set of alternative test sets, and schedule it in a way that evenly balances the resource usage, and ultimately reduce the test application time. Furthermore, we propose a novel approach that groups the cores and assigns higher priority to those with smaller number of alternate test sets. In addition, we also e ...

Keywords: resource balancing, system-on-a-chip test scheduling, test sets selection

26 Efficient Wrapper/TAM Co-Optimization for Large SOCs

V. Iyengar, K. Chakrabarty, E. Marinissen
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(225.35 KB) Publisher Site Additional Information: full citation, abstract, citings

Core test wrappers and test access mechanisms (TAMs) are importantcomponents of a system-on-chip (SOC) test architecture.Wrapper/TAM co-optimization is necessary to minimize the SOC testingtime. Most prior research in wrapper/TAM design has addressedwrapper design and TAM optimization as separate problems, therebyleading to results that are sub-optimal. We present a fast heuristictechnique for wrapper/TAM co-optimization, and demonstrate itsscalability for several industrial SOCs. This extends r ...

27 Effective Software Self-Test Methodology for Processor Cores

N. Kranitis, A. Paschalis, D. Gizopoulos, Y. Zorian
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(284.27 KB) Additional Information: full citation, abstract
Publisher Site

Software self-testing for embedded processor coresbased on their instruction set, is a topic of increasinginterest since it provides an excellent test resourcepartitioning technique for sharing the testing task ofcomplex Systems-on-Chip (SoC) between slow,inexpensive testers and embedded code stored in memorycores of the SoC. We introduce an efficient methodologyfor processor cores self-testing which requires knowledgeof their instruction set and Register Transfer (RT) leveldescription. Compared ...

28 Improving Compression Ratio, Area Overhead, and Test Application Time for System-on-a-Chip Test Data Compression/Decompression

P. Gonciari, B. Al-Hashimi, N. Nicolici
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(162.69 KB) Additional Information: full citation, abstract, citings
Publisher Site

This paper proposes a new test data compression/decompression method for systems-on-a-chip. Themethod is based on analyzing the factors that influencetest parameters: compression ratio, area overhead and testapplication time. To improve compression ratio, the newmethod is based on a Variable-length Input Huffman Coding(VIHC), which fully exploits the type and length of the patterns,as well as a novel mapping and reordering algorithmproposed in a pre-processing step. The new VIHC algorithmis comb ...

29 Test Planning and Design Space Exploration in a Core-Based Environment

E. Cota, L. Carro, M. Lubaszewski, A. Orailoglu
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(133.63 KB) Additional Information: full citation, abstract, citings
Publisher Site

This paper proposes a comprehensive model for testplanning in a core-based environment. The main contributionof this work is the use of several types of TAMs and theconsideration of different optimization factors (area, pinsand test time) during the global TAM and test schedule definition.This expansion of concerns makes possible an efficientyet fine-grained search in the huge design space ofa reuse-based environment. Experimental results clearlyshow the variety of trade-offs that can be explore ...

30 Cellular and Cryptographic Applications: FPGA implementation of neighborhood-of-four cellular automata random number generators

Barry Shackleford, Motoo Tanaka, Richard J. Carter, Greg Snider
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Full text available: pdf(565.95 KB) Additional Information: full citation, abstract, references

Random number generators (RNGs) based upon neighborhood-of-four cellular automata (CA) with asymmetrical, non-local connections are explored. A number of RNGs that pass Marsaglia's rigorous Diehard suite of random number tests have been discovered. A neighborhood size of four allows a single CA cell to be implemented with a four-input lookup table and a one-bit register which are common building blocks in popular field programmable gate arrays (FPGAs). The investigated networks all had periodic ...

Keywords: FPGA, cellular automata, random number generator

31 Reformatting Test Patterns for Testing Embedded Core Based System Using Test

Access Mechanism (TAM) Switch

Subhayu Basu, Debdeep Mukhopadhay, Dipanwita Roychoudhury, Indranil Sengupta, Sudipta Bhawmik

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(143.13 KB) Publisher Site

Additional Information: full citation, abstract

In the present paper a new algorithm for reformatting the test vector of System On Chip (SOC) with Test Access Mechanism (TAM) has been proposed. Exhaustive experimentation has been done by employing random reformatted test vectors to a variety of SOCs, constructed with the ISCAS sequential benchmark circuits. For a limited number of input pins, which has been provided for testing the SOC, the proposed algorithm reduces drastically the test-time as well as the hardware.

Keywords: Test Access Mechanism, Data acyclic graph, Test patterns, Test time, System-on-Chip

32 Design of An On-Chip Test Pattern Generator Without Prohibited Pattern Set (PPS)

Niloy Ganguly, Biplab K. Sikdar, P P. al Chaudhuri

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(333.07 KB) Publisher Site

Additional Information: full citation, abstract

This paper reports the design of a T est P attern Generator (TPG) for V LSI circuits. The on-chip TPG is so designed that it generates test patterns while avoiding generation of a given Prohibited Pattern Set (PPS). The design ensures desired pseudo-random quality of the test patterns generated.The experimental results confirm high quality of randomness while ensuring fault coverage close to the figures achieved with a typical Pseudo Random Pattern Generator (PRPG) designed around maximal length ...

33 A Partitioning and Storage Based Built-In Test Pattern Generation Method for Scan Circuits

Irith Pomeranz, Sudhakar M. Reddy

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(129.50 KB) Publisher Site

Additional Information: full citation, abstract

We describe a built-in test pattern generation method for scan circuits.The method is based on partitioning and storage of test sets.Under this method,a precomputed test set is partitioned into several sets containing values of different primary inputs or state variables.The on-chip test set is obtained by implementing the Cartesian product of the various sets.The sets are reduced as much as possible before they are stored on-chip in order to reduce the storage requirements and the test applicat ...

34 On Test Scheduling for Core-Based SOCs

Sandeep Koranne

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(180.64 KB) Publisher Site

Additional Information: full citation, abstract, citings

We present a mathematical model for the problem of scheduling tests for core-based

system-on-chip (SOC) VLSI designs. Given a set of tests for each core in the SOC and a set of test resources (e.g., test access mechanisms (TAM)), we determine the test plan for the application of the tests to the SOC. Test planning in this paper refers to the combined activities of test access architecture partitioning and test scheduling. These activities must be performed in conjunction as the choice of the tes ...

35 Session 9A: System level test and reliability: The design and optimization of SOC test solutions

Erik Larsson, Zebo Peng, Gunnar Carlsson

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(182.66 KB) Additional Information: full citation, abstract, references, index terms

We propose an integrated technique for extensive optimization of the final test solution for System-on-Chip using Simulated Annealing. The produced results from the technique are a minimized test schedule fulfilling test conflicts under test power constraints and an optimized design of the test access mechanism. We have implemented the proposed algorithm and performed experiments with several benchmarks and industrial designs to show the usefulness and efficiency of our technique.

36 Von Neumann hybrid cellular automata for generating deterministic test sequences

D. Kagaris, S. Tragoudas

July 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 3

Full text available: pdf(143.85 KB) Additional Information: full citation, abstract, references, index terms

We propose an on-chip test pattern generator that uses an one-dimensional cellular automaton (CA) to generate either a precomputed sequence of test patterns or pairs of test patterns for path delay faults. To our knowledge, this is the first approach that guarantees successful on-chip generation of a given test pattern sequence (or a given test set for path delay faults) using a finite number of CA cells. Given a pair of columns (Cu, C

Keywords: built-in self-test (BIST), cellular automata, test pattern generation

37 Intrinsic response for analog module testing using an analog testability bus

Chauchin Su, Yue-Tsang Chen, Shyh-Jye Jou

April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2

Full text available: pdf(277.66 KB) Additional Information: full citation, abstract, references, index terms

A parasitic effect removal methodology is proposed to handle the large parasitic effects in analog testability buses. The removal is done by an on-chip test generation technique and an intrinsic response extraction algorithm. On-chip test generation creates test signals on-chip to avoid the parasitic effects of the test application bus. The intrinsic response extraction cross-checks and cancels the parasitic effects of both test application and response observation paths. The tests using bo ...

Keywords: analog testability bus, analog testing, boundary scan, design for testability, intrinsic response

38 An integrated system-on-chip test framework

E. Larsson, Z. Peng

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(139.63 KB) Additional Information: full citation, references, citings, index terms

39 Embedded tutorial: TRP: integrating embedded test and ATE

Y. Zorian, P. Prinetto, J. Teixeira, I. Teixeira, C. Pereira, O. Dias, J. Semiao, P. Muhmenthaler, W. Radermacher

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(67.84 KB) Additional Information: full citation, references, index terms

40 Synthesis of single-output space compactors with application to scan-based IP cores

Bhargab B. Bhattacharya, Alexej Dmitriev, Michael Gössel, Krishendu Chakrabarty

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(287.16 KB) Additional Information: full citation, abstract, references, index terms

This paper addresses the problem of space compaction of test responses of combinational and scan-based sequential circuits. It is shown that given a precomputed test set T, the test responses at the functional outputs of the given circuit-under-test (CUT) can be compacted to a single periodic output, with guaranteed zero-aliasing. The method is independent of the fault model and the structure of the CUT, and uses only the knowledge of the test set T and the corresponding fault-free response ...

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41 Cellular automata as a built in self test structure

Biplab K. Sikdar, Debesh K. Das, Vamsi Boppana, Cliff Yang, Sobhan Mukherjee, P. Pal Chaudhuri

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(296.56 KB) Additional Information: full citation, abstract, references, index terms

This paper presents an efficient BIST solution for VLSI circuit testing based on GF(2p) CA (Cellular automata on an extended Galois Field). The novel architecture of GF(2p)) CA permits the BIST structure to be highly customized to the circuit under test (CUT). A methodology has been proposed to optimize the design of GF(2p) CA structure to maximize the fault coverage in a given CUT. In addition, an innovative scheme based on logic folding is presented to reduce the BIST overhead and make it ...

42 Optimal test access architectures for system-on-a-chip

Krishnendu Chakrabarty

January 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 1

Full text available: pdf(197.95 KB) Additional Information: full citation, abstract, references, citings, index terms

Test access is a major problem for core-based system-on-a-chip (SOC) designs. Since embedded cores in an SOC are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. An efficient test access architecture should also reduce test cost by minimizing test application time. We address several issues related to the design of optimal test access architectures that minimize testing time., including the assignment of cores to t ...

43 Session 8D: embedded tutorial: Test of future system-on-chips

Yervant Zorian, Sujit Dey, Michael J. Rodgers

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(140.88 KB) Additional Information: full citation, abstract, references, citings

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. Being able to rapidly develop, manufacture, test, debug and verify complex SOCs is crucial for the continued success of the electronics industry. This growth is expected to continue full force at least for the next decade, while making possible the production of

multimillion transistor chips. However, to mak ...

44 Session 9D: new approaches to at-speed BIST and diagnosis: Diagnosis of interconnect faults in cluster-based FPGA architectures

Ian Harris, Russell Tessier

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(60.64 KB) Additional Information: full citation, abstract, references, citings

Fault diagnosis has particular importance in the context of field programmable gate arrays (FPGAs) because faults can be avoided by reconfiguration at almost no real cost. Cluster-based FPGA architectures, in which several logic blocks are grouped together into a coarse-grained logic block, are rapidly becoming the architecture of choice for major FPGA manufacturers. The high density interconnect found within clusters greatly complicates the problem of FPGA diagnosis. We propose a technique for ...

45 Verification of configurable processor cores

Marinés Puig-Medina, Gülbin Ezer, Pavlos Konas

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(79.05 KB) Additional Information: full citation, abstract, references, citings

This paper presents a verification methodology for configurable processor cores. The simulation-based approach uses directed diagnostics and pseudo-random program generators both of which are tailored to specific processor instances. A configurable and extensible test-bench serves as the framework for the verification process and offers components necessary for the complete SOC verification. Coverage analysis provides an evaluation of how well a specific design has been exercised, of the br ...

Keywords: co-simulation, configurable processor cores, coverage analysis, design verification, system-on-chip, test generation

46 Design of system-on-a-chip test access architectures under place-and-route and power constraints

Krishnendu Chakrabarty

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(108.28 KB) Additional Information: full citation, abstract, references, citings, index terms

Test access is a difficult problem encountered in the testing of core-based system-on-a-chip (SOC) designs. Since embedded cores in an SOC are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. We propose test access architectures based on integer linear programming (ILP) that incorporate place-and-route constraints arising from the functional interconnections between cores, as well as system-level constraint ...

47 Embedded hardware and software self-testing methodologies for processor cores

Li Chen, Sujit Dey, Pablo Sanchez, Krishna Sekar, Ying Cheng

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(103.87 KB) Additional Information: full citation, abstract, references, citings, index terms

At-speed testing of GHz processors using external testers may not be technically and economically feasible. Hence, there is an emerging need for low-cost, high-quality self-test methodologies, which can be used by processors to test themselves at-speed. Currently, Built-In Self-Test (BIST) is the primary self-test methodology available and is widely used

for testing embedded memory cores. In this paper, we report our experiences in applying a commercial BIST methodology to two processor cor ...

48 Improved fault diagnosis in scan-based BIST via superposition
Ismet Bayraktaroglu, Alex Orailoğlu
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(80.86 KB) Additional Information: full citation, abstract, references, citings, index terms

An improved approach for diagnosis of scan-based BIST designs is proposed. The enhancement in diagnosis is achieved by utilizing the superposition principle. Scan cells are partitioned pseudorandomly for observation and the ones provably fault free are removed from the potentially faulty list. Diagnostic resolution is improved by a novel application of the superposition principle, resulting in significant reductions in diagnosis time.

49 Self-test methodology for at-speed test of crosstalk in chip interconnects
Xiaoliang Bai, Sujit Dey, Janusz Rajski
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(113.37 KB) Additional Information: full citation, abstract, references, citings, index terms

The effect of crosstalk errors is most significant in high-performance circuits, mandating at-speed testing for crosstalk defects. This paper describes a self-test methodology that we have developed to enable on-chip at-speed testing of crosstalk defects in System-on-Chip interconnects. The self-test methodology is based on the Maximal Aggressor Fault Model [13], that enables testing of the interconnect with a linear number of test patterns. To enable self-testing of the interconnects, we h ...

50 A sigma-delta modulation based BIST scheme for mixed-signal circuits
Jiun-Lang Huang, Kwang-Ting Cheng
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(117.31 KB) Additional Information: full citation, references, citings

51 A BIST scheme for on-chip ADC and DAC testing
Jiun-Lang Huang, Chee-Kian Ong, Kwang-Ting Cheng
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(114.67 KB) Publisher Site Additional Information: full citation, references, citings, index terms

52 Built-in generation of weighted test sequences for synchronous sequential circuits
Irith Pomeranz, Sudhakar M. Reddy
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(66.38 KB) Publisher Site Additional Information: full citation, references, index terms

53 An on chip ADC test structure
Yun-Che Wen, Kuen-Jong Lee
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(118.24 KB) Additional Information: full citation, references, index terms
Publisher Site

54 Yield improvement and repair trade-off for large embedded memories
Yervant Zorian
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(25.85 KB) Additional Information: full citation, citings, index terms
Publisher Site

Keywords: BIST, DFM, Yield improvement, silicon repair

55 A methodology for the verification of a "system on chip"
Daniel Geist, Giora Biran, Tamara Arons, Michael Slavkin, Yvgeny Nustov, Monica Farkas, Karen Holtz, Andy Long, Dave King, Steve Barret
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(63.75 KB) Additional Information: full citation, references, citings, index terms

Keywords: systems on chip, test and debugging, verification

56 Built-in test sequence generation for synchronous sequential circuits based on loading and expansion of test subsequences
Irith Pomeranz, Sudhakar M. Reddy
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(48.24 KB) Additional Information: full citation, references, citings, index terms

57 Digital detection of analog parametric faults in SC filters
Ramesh Harjani, Bapiraju Vinnakota
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(110.43 KB) Additional Information: full citation, references, citings, index terms

58 On-chip transient current monitor for testing of low-voltage CMOS IC
V. Stopjaková, H. Manhaeve, M. Sidiropulos
January 1999 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(378.04 KB) Additional Information: full citation, citings, index terms

59 A digital partial built-in self-test structure for a high performance automatic gain control circuit
A. Lechner, J. Ferguson, A. Richardson, B. Hermes
January 1999 **Proceedings of the conference on Design, automation and test in Europe**
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60 Design for testability method for CML digital circuits
Bernard Antaki, Yvon Savaria, Saman M. I. Adham, Nanhan Xiong
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